

## CLAIMS

What is claimed is:

1. A method for designing a cell-based application specific integrated circuit (ASIC) device, said method comprising:

reserving metal layer M1 power supply bus when developing a bus structure ASIC device image;

grouping circuit macros of like power supply voltages into respective logic blocks;

synthesizing said logic blocks using sub-libraries corresponding to voltages for said logic blocks; and

adding power supply bus for said supply voltage to metal layer M1 in said logic blocks.

1        2.        The method of Claim 1, wherein said method further includes separating said logic  
2        blocks of different voltages via a filler cell.

1        3.        The method of Claim 1, wherein one of said logic blocks contains a custom  
2        intellectual property macro.

1        4.        The method of Claim 1, wherein said method further includes utilizing a level  
2        convertor having multiple power supply voltages.

1        5.        A computer program product residing on a computer usable medium for designing  
2        a cell-based application specific integrated circuit (ASIC) device, said computer program  
3        product comprising:

4                    program code means for reserving metal layer M1 power supply bus when  
5                    developing a bus structure ASIC device image;

6                    program code means for grouping circuit macros of like power supply  
7                    voltages into respective logic blocks;

8                    program code means for synthesizing said logic blocks using sub-libraries  
9                    corresponding to voltages for said logic blocks; and

10                   program code means for adding power supply bus for said supply voltage  
11                   to metal layer M1 in said logic blocks.

1        6.        The computer program product of Claim 5, wherein said computer program product  
2        further includes program code means for separating said logic blocks of different voltages  
3        via a filler cell.

1        7.        The computer program product of Claim 5, wherein one of said logic blocks  
2        contains a custom intellectual property macro.

1        8.        The computer program product of Claim 5, wherein said computer program product  
2        further includes program code means for utilizing a level convertor having multiple power  
3        supply voltages.

1        9.        A system for designing a cell-based application specific integrated circuit (ASIC)  
2        device, said system comprising:

3                    program code means for reserving metal layer M1 power supply bus when  
4                    developing a bus structure ASIC device image;

5                    program code means for grouping circuit macros of like power supply  
6                    voltages into respective logic blocks;

7                    program code means for synthesizing said logic blocks using sub-libraries  
8                    corresponding to voltages for said logic blocks; and

9                    program code means for adding power supply bus for said supply voltage  
10                    to metal layer M1 in said logic blocks.

1        10.     The system of Claim 9, wherein said system further includes means for separating  
2        said logic blocks of different voltages via a filler cell.

1        11.     The system of Claim 9, wherein one of said logic blocks contains a custom  
2        intellectual property macro.

1        12.     The system of Claim 9, wherein said system further includes means for utilizing a  
2        level convertor having multiple power supply voltages.